87

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,096	06/22/2001	Lauren B. Wenzl	X-662 US	7929

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EXAMINER	
ZHEN, LI B	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,096	WENZL, LAUREN B.	
	Examiner	Art Unit	
	Li B. Zhen	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 15 are pending in the current application.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/01/2005 has been entered.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Drawings

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 8 and 12 recites "implements an interface" [claim 8, line 16 and claim 12, line 14]. It is unclear as to which interface this limitation is referring to, i.e., interface for an electronic device, control interface, communication interface or hardware interface.

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 1 – 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Currently amended claims recite the new limitations: "second communication interface adapted to request a bitstream from the electronic device responsive to a signal from the second control interface" [claim 1, lines 22 – 24]; "configure the second configurable hardware interface to implement an interface compatible with the driver on the first configurable hardware interface" [claim 1, lines 25 – 27]; "configuring a second PLD in the peripheral device with a second bitstream that implements an interface compatible with the driver implemented in the first PLD" [claim 8, lines 15 – 16]; "configuring a second PLD in the first device with a second bitstream that implements an interface compatible with a driver implemented in the first PLD" [claim 12, lines 13 – 14]. Although applicant's specification discloses configurable hardware interfaces in both the host and peripheral devices [p. 4, paragraph 0011], applicant's specification does not disclose a peripheral device requesting a bitstream from the host device and configuring the hardware interface on the peripheral device with a bitstream to implement an interface that is compatible with the driver implemented on the host device. Further down on the same page, applicant

discloses the PLD of the configurable hardware interface can be configured to facilitate communication between any two devices [p. 4, paragraph 0011]. Only one of the hardware interfaces is configured to provide communication between any two devices; however, the currently presented claims requires both hardware interfaces [host and peripheral] to be configured before the two devices can communicate. Throughout the specification, applicant discloses configuring the hardware interface on the host device with a bitstream to implement a driver of the peripheral device [p. 2, lines 28-30; p. 3, lines 3-6, 12-16; p. 4, lines 3-5; p. 8, lines 13-15, 21-22; p. 9, lines 25-27] and the peripheral device waits for commands from the host device if the host device can access the needed driver [p. 3, paragraph 0009 and p. 9, paragraph 0027]. Examiner was unable to locate any description of the communication interface in the peripheral device requesting a bitstream from the host device and configuring a second PLD in the peripheral device with a second bitstream that implements an interface compatible with the driver implemented in the first PLD. Therefore, the applicant fails to disclose the newly recited limitations in the specification as filed.

9. Claims 1 – 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, the specification does not teach a communication interface in the peripheral device requesting a bitstream from the host device and configuring a second PLD in the peripheral device with a second bitstream that implements an interface compatible with the driver implemented in the first PLD. The specification discloses configuring a hardware interface in the host device with a bitstream to implement a driver of the peripheral device [p. 2, lines 28-30; p. 3, lines 3-6, 12-16; p. 4, lines 3-5; p. 8, lines 13-15, 21-22; p. 9, lines 25-27] and the peripheral device waits for commands from the host device [p. 3, paragraph 0009 and p. 9, paragraph 0027]. When the hardware interface in the host device is configured to implement a driver for the peripheral device, the host device and the peripheral device would be able to

communicate with each other through the hardware interface. It not implicit nor inherent to one of ordinary skill in the art as to why the peripheral device would need additional information from the host device to implement an interface for its own driver. In addition, the specification does not implicitly or inherently disclose how the host device would contain bitstream that implements an interface compatible with a driver of the peripheral device.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent NO. 6,477,611 to Chang [cited in the previous office action] in view of U.S. Patent NO. 6,754,723 to Kato.**

12. As to claim 1, Chang teaches the invention substantially as claimed including an interface [CAP interface circuit 30, Fig. 1; col. 4, lines 62 – 67] for an electronic device [computer 11, Fig. 1; col. 4, lines 47 – 61] being coupled to a peripheral device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32], the interface including:

a first configurable hardware interface [CAP interface circuit 30, Fig. 1; col. 4, line 62 – col. 5, line 17], wherein the configurable hardware interface is resident in the electronic device includes:

a first programmable logic device (PLD) [FPGA 31, Fig. 1; col. 5, lines 3 – 17];

a first memory coupled to the first PLD [FPGA configuration buffer 32, Fig. 1; col. 4, lines 62 – 67];

a first control interface for controlling the first PLD and the first memory [CAP interface circuit 30; col. 4, line 62 – col. 5, line 18]; and

a first communication interface [FPGA 31 is electrically connected to CAP I/O bus 15 through a connector 34; col. 4, line 62 – col. 5, line 2] for receiving information from the peripheral device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32] and enabling the first control interface [at least one conductor of CAP I/O Bus 15, which may be called IN_CAP conductor (or line or pin) 17, is used to communicate the identification number for module 12 from module 12 to computer 11, Fig. 1; col. 5, lines 30 – 43], the first communication interface adapted to request a bitstream from the peripheral device responsive to a signal from the first control interface [If the configuration information for module 12 is not located in Domain "A" (block 75), a new ID flag is set to a logic level 1 (block 85), and the two most significant bits of the identification number are examined by CPU 20 in block 87 to determine if the configuration information is located in Domain "B", module 12; col. 7, line 55 – col. 8, line 5]; and

a first storage component [computer memory 33, Fig. 1; col. 6] for storing a bitstream that configures the first configurable hardware interface to implement a driver of the external device [CAP Bus computer memory 33 includes three databases...FIG. 2. A first database, referred to as Domain "A" CAP Bus Database 51, has i entries each having a bus logic FPGA image file 52 and a device driver 53. A second database, referred to as Protocol Bus Database 55, has j entries each having a bus logic FPGA image file 56 and a protocol driver 57; col. 6, lines 21 – 46];

a second configurable hardware interface, wherein the configurable hardware interface is resident in the peripheral device [CAP compatible module 12; col. 5, lines 18 – 30] and includes:

a second PLD [CAP line and I/O control circuit 40 may be any of the various line control circuits; col. 5, lines 18 – 29]:

a second memory coupled to the second PLD [CAP module memory 42; col. 5, lines 18 – 29]; and

a second control interface for controlling the second PLD and the second memory [CAP line and I/O control circuit 40; col. 5, lines 18 – 30].

13. Although Chang teaches the invention substantially, Chang does not specifically teach the second communication interface requesting a bitstream from the electronic device and configuring the second configurable hardware interface to implement an interface compatible with the driver on the first configurable hardware interface.

However, Kato teaches interface for an electronic device being coupled to a peripheral device [col. 3, lines 53 – 65], the electronic device including a first configurable hardware interface [option interface 112, Fig. 1; col. 3, lines 18 - 46], the peripheral device including a second configurable hardware interface [option interface 210, Fig. 1; col. 3, lines 18 – 46], configuring the first configurable hardware interface to implement a driver of the external device [download means downloads the firmware of the printer...from the HDD to the memory of the device, and the firmware is updated; col. 3, line 66 – col. 4, line 20]; the second communication interface adapted to request a bitstream from the electronic device responsive to a signal from the second control interface [download means downloads the firmware of...the mailbox from the HDD to the memory of the device, and the firmware is updated; col. 4, lines 1 – 20]; and a second storage component for storing a plurality of bitstreams [firmware for the part of the printer 100 requiring modification or the firmware of part of the mailbox 200 requiring modification is stored in ROM (106 or 204); col. 5, lines 3 – 16] that configure the second configurable hardware interface to implement an interface compatible with the driver on the first configurable hardware interface [col. 5, lines 1 – 16].

14. It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply the teaching of requesting a bitstream from the electronic device and configuring the second configurable hardware interface to implement an interface compatible with the driver on the first configurable hardware interface as taught by Kato

to the invention of Chang because this provides a system and method capable of interconnecting even combinations other than devices for which such connection was considered beforehand in a system comprising a device and at least one peripheral device connected thereto [col. 2, lines 21 - 25 of Kato]. In addition, this allows incompatible devices lacking functions to be automatically updated to provide new functions and compatibility so that it is unnecessary to produce an entirely new product for these functions, and total management cost is reduced [col. 7, lines 5 - 10 of Kato].

15. As to claim 2, Chang as modified teaches at least one of the first and second storage components includes volatile memory [computer memory 33, Fig. 1; col. 6 and col. 4, lines 47 – 52 of Chang].

16. As to claim 3, Chang as modified teaches at least one of the first and second storage components includes static random access memory [computer memory 33, Fig. 1; col. 6 and col. 4, lines 47 – 52 of Chang].

17. As to claim 4, Chang as modified teaches at least one of the first and second communication interfaces includes one of a universal serial bus, a parallel port connector, a serial port connector [CAP I/O bus 15 through a connector 34; col. 5, lines 1 – 2 of Chang], and a small computer system interface (SCSI).

18. As to claim 5, Chang as modified teaches at least one of the first and second communication interfaces establish synchronous communication between the electronic device and the peripheral device [establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 15 – 30 of Chang].

19. As to claim 6, Chang as modified teaches at least one of the first and second memories include at least one lookup table [CAP Bus computer memory 33 includes three databases; col. 6, lines 23 – 46 of Chang].

20. As to claim 7, Chang as modified teaches including at least one of an Ethernet interface, a modem interface, and a custom interface for communicating with the peripheral device [Any conventional communication device compatible with standard protocol port 24, such as an analog modem 27, may be electrically connected with connector 23 to allow communication with external computers and networks such as a server 28 accessible through the Internet; col. 4, lines 52 – 61 of Chang].

21. As to claim 8, Chang as modified teaches a method of facilitating communication between two devices [establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 15 – 30 of Chang], the method comprising:

identifying a host device [computer 11, Fig. 1; col. 4, lines 47 – 61 of Chang], from the two devices, that controls communication between the two devices [the device driver is executed, thereby establishing communication operation between computer 11 and module 12; col. 7, lines 39 – 54 of Chang];

identifying a peripheral device that accepts commands from the host device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32 of Chang];

storing a plurality of bitstreams in the host device, the plurality of bitstreams corresponding to drivers [CAP Bus computer memory 33 includes three databases...FIG. 2. A first database, referred to as Domain "A" CAP Bus Database 51, has i entries each having a bus logic FPGA image file 52 and a device driver 53. A second database, referred to as Protocol Bus Database 55, has j entries each having a bus logic FPGA image file 56 and a protocol driver 57; col. 6, lines 21 – 46 of Chang]; and

determining whether one of the drivers is a driver of the peripheral device [If the configuration information for module 12 is not located in Domain "A" (block 75), col. 7, lines 55 – 67; If the configuration information for module 12 is not located in Domain "A" or Domain "B" as determined in block 87, col. 8, lines 6 – 8 of Chang],

wherein if on of the drivers is the driver of the peripheral device, then selecting that bitstream corresponding to the driver of the peripheral device [block 77 the corresponding CAP Bus logic FPGA image file, and device driver for ID.sub.x are retrieved from CAP Bus computer memory 33 and loaded into FPGA configuration buffer 32; col. 7, lines 39 – 54 of Chang],

otherwise, directing the host device to receive a first bitstream from the peripheral device [configuration information is retrieved from the location corresponding to the identification number from one of a plurality of locations including the first device, the second device and an external source; col. 3, lines 54 – 63 of Chang];

configuring a first programmable logic device (PLD) [FPGA 31, Fig. 1; col. 5, lines 3 – 17 of Chang] in the host device with the first bitstream to implement the driver of the peripheral device [FPGA 31 then configures the CAP Bus in accordance with the contents of FPGA configuration buffer 32, as described in block 79, and, in block 80, the device driver is executed, thereby establishing communication operation between computer 11 and module 12; col. 7, lines 39 – 54 of Chang]; and

configuring a second PLD in the peripheral device with a second bitstream that implements an interface compatible with the driver implemented in the first PLD [download means downloads the firmware of...the mailbox from the HDD to the memory of the device, and the firmware is updated; col. 4, lines 1 – 20 of Kato]. As to the motivation for combining Chang with Kato, see the rejection to claim 1 above.

22. As to claim 9, Chang as modified teaches storing a plurality of designations [locations] in the first PLD, wherein each designation corresponds to one of the plurality of bitstreams [configuration information necessary to configure FPGA 31 to interface correctly with module 12 is available in one of four locations: onboard computer 11 in CAP Bus memory 33 (which shall be referred to as Domain "A"); onboard module 12 in CAP module memory 42 (which shall be referred to as Domain "B"); col. 5, line 65 – col. 6, line 13 of Chang], wherein determining includes searching the plurality of designations [block 75 and block 87, Fig. 5A; col. 8, lines 6 – 8 of Chang].

23. As to claim 10, this is similar in scope to claim 6; therefore, it is rejected for the same reasons as claim 6 above.

24. As to claim 11, Chang as modified teaches each designation includes an address for one of the plurality of bitstreams stored in the host device [CAP I/O Bus specification to find the entry in CAP Bus ID directory 60 whose secondary memory pointer corresponds to the bus logic FPGA image files, device driver, and/or protocol driver needed for module 12; col. 6, lines 56 – 65 of Chang], and wherein selecting includes accessing an address in the host device for the first bitstream to implement the driver of the peripheral device [retrieving that information from the location specified by the identification, reconfiguring the I/O Bus of computer 11 to be compatible with the I/O Bus configuration of external module 12, and establishing communication between the I/O buses of computer 11 and module 12; col. 7, lines 16 – 30 of Chang].

25. As to claim 12, Chang as modified teaches a method for configuring an interface, comprising:

communicating a designation of a driver [pass an identification number from module 12 to computer 11; col. 4, lines 32 – 47 of Chang] from a first device [modules such as so-called add-in boards or peripherals that add significant functionality to a general-purpose computer, col. 1, lines 33 – 45; external module 12, Fig. 1, col. 4, lines 16 – 32 of Chang] to a second device [computer 11, Fig. 1; col. 4, lines 47 – 61 of Chang];

determining at the second device whether a first configuration bitstream associated with the designation of the driver is stored in storage of the second device [block 77 the corresponding CAP Bus logic FPGA image file, and device driver for ID.sub.x are retrieved from CAP Bus computer memory 33 and loaded into FPGA configuration buffer 32; col. 7, lines 39 – 54 of Chang];

communicating a bitstream request from the second device to the first device in response to the first bitstream being absent from the storage [If the configuration information for module 12 is not located in Domain "A" (block 75), a new ID flag is set to

a logic level 1 (block 85), and the two most significant bits of the identification number are examined by CPU 20 in block 87 to determine if the configuration information is located in Domain "B", module 12; col. 7, line 55 – col. 8, line 5 of Chang];

transmitting, in response to the bitstream request, the first bitstream from the first device to the second device [in block 91, the CAP Bus logic FPGA image file and device driver for ID.sub.x are retrieved from CAP module memory 42 and transferred to and loaded into FPGA configuration buffer 32; col. 7, line 55 – col. 8, line 5 of Chang];

configuring a first programmable logic device (PLD) on the second device with the first bitstream [remaining process for configuring CAP I/O Bus is the same as when the configuration information was obtained from Domain "A"; col. 7, line 40 – col. 8, line 6 of Chang]; and

configuring a second PLD in the first device with a second bitstream that implements an interface compatible with a driver implemented in the first PLD [download means downloads the firmware of...the mailbox from the HDD to the memory of the device, and the firmware is updated; col. 4, lines 1 – 20 of Kato]. As to the motivation for combining Chang with Kato, see the rejection to claim 1 above.

26. As to claim 13, Chang as modified teaches in response to the first bitstream being present in the storage, reading the first bitstream from the storage and configuring the first PLD on the second device [determine if the configuration information is located in Domain "A". If so, in block 77 the corresponding CAP Bus logic FPGA image file, and device driver for ID.sub.x are retrieved from CAP Bus computer memory 33 and loaded into FPGA configuration buffer 32; col. 7, lines 40 – 55 of Chang].

27. As to claim 14, Chang as modified teaches storing the first bitstream received from the first device in the storage on the second device [the CAP Bus logic FPGA image file and device driver for ID.sub.x are retrieved from CAP module memory 42 and transferred to and loaded into FPGA configuration buffer 32; col. 7, line 55 – col. 8, line 5 of Chang].

28. As to claim 15, Chang as modified teaches storing a plurality of configuration bitstreams and associated designation of drivers in the storage [CAP Bus computer memory 33 includes three databases...FIG. 2. A first database, referred to as Domain "A" CAP Bus Database 51, has i entries each having a bus logic FPGA image file 52 and a device driver 53. A second database, referred to as Protocol Bus Database 55, has j entries each having a bus logic FPGA image file 56 and a protocol driver 57; col. 6, lines 21 – 46 of Chang].

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent NO. 6,574,588 to Shapiro et al. teaches a peripheral device that integrally provides a program relating to the peripheral device.

U.S. Patent NO. 6,539,438 to Ledzius et al. teaches a reconfigurable computing system for interfacing a plurality of application programs running on a host system to one or more hardware objects.

U.S. Patent NO. 6,249,825 and 6,012,103 to Sartore et al. teaches a system for reconfiguring a peripheral device having a first configuration connected by a computer bus and a port to a host computer.

U.S. Patent NO. 6,145,020 to Barnett teaches an enhanced peripheral controller communicating between a microcontroller and multiple peripherals.

U.S. Patent NO. 5,915,106 to Ard teaches a disk driver emulator attached to a general-purpose computer via a SCSI bus.

U.S. Patent NO. 5,379,382 to Work et al. teaches a peripheral controller for connecting a peripheral device to a computer system.

CONTACT INFORMATION

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on 571-272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2194

lbz

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